C/M 11-14-02

S/N 09/881,472 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ramandeep S. Sawhney	Examiner:	Ly Pham
Serial No.:	09/881,472	Group Art Unit:	2818
Filed:	June 14, 2001	Docket:	303.729US1
Title:	SEMICONDUCTOR MEMORY WITH WORDLINE TIMING		

T/A A Mackey 12-2-02

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

This paper is in response to the Office Action mailed on August 14, 2002. Please amend the above-identified patent application as follows.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 43 and 49, and addition of new claims 70-88. The specific amendments to individual claims are detailed in the following marked up set of claims.

43. (Amended) A timing circuit, comprising:

an input adapted to receive at least one input signal, the at least one input signal including [an] a sense amplifier isolation signal; and

an output connected to an address decoder, wherein the timing circuit activates the address decoder based on the at least one input signal.

49. (Amended) A timing circuit connected to a wordline decoder of a first memory array, the timing circuit comprising:

an input adapted to receive at least one input signal, the at least one input signal including [an] a sense amplifier isolation signal connected to a sense amplifier for a second memory array; and

an output connected to the wordline decoder, wherein the timing circuit activates the wordline decoder based on the at least one input signal.